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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,726	03/12/2001	Peyman Hadizad	ONS00181	7690

7590 12/04/2002

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	PAPER NUMBER
2813	4

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,726	HADIZAD ET AL.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *4* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Election filed 9/25/02, in Paper No. 3.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al ('446).

In reference to claim 1, Gardner teaches a component comprising:

A semiconductor layer having a trench with first and second sides, a portion of the semiconductor layer having a first conductivity type and a first charge density (Fig.3 (46) and Col.6, lines:45-50- teaching to dope the substrate therefore forming a charge density);

A control electrode in the trench (Fig. 5 (54));

A channel region in the semiconductor layer and adjacent to the trench (Col.8, lines: 34-36); and

A first region in the semiconductor layer, having a second conductivity type, and having a second charge density balancing the first charge density (Fig.12 (60 and 66)- an LDD implant

is of a second type of conductivity to the substrate at a different concentration, thus it has a different charge density the same is true for a heavily doped drain).

In reference to claim 2, Gardner teaches wherein:

The semiconductor layer has a first surface and a second surface (Fig. 1 (40) top and bottom);

A first portion of the first region is at the first side of the trench and extends along a height of the semiconductor layer from the first surface of the semiconductor layer toward the second surface of the semiconductor layer (Fig.12 (60)); and

A second portion of the first region is at the second side of the trench and extends along the height of the semiconductor layer from the first surface toward the second surface (Fig.12 (60)).

In reference to claim 3, Gardner teaches wherein the first region is discontinuous (Fig.12 (60)).

In reference to claim 4, Gardner teaches wherein the first portion of the first region is discontinuous (Fig.12(60)).

In reference to claim 5, Gardner teaches wherein the first region is continuous (Fig.12 (66)).

In reference to claim 6, Gardner teaches wherein the first region is continuous from the first surface toward the second surface (Fig.12 (66)).

In reference to claim 7, Gardner teaches wherein the first region is continuous with the first surface (Fig.12 (66)); and

The trench is in the second surface (Fig.3 (46)).

In reference to claim 8, Gardner teaches wherein the channel region is between the first and second portions of the first region (Col.8, lines: 34-36).

In reference to claim 9, Gardner teaches further comprising an electrically insulative layer in the trench between the semiconductor layer and the control electrode (Fig.10 (50)).

In reference to claim 10, Gardner teaches wherein the control electrode is located only in the trench (Fig.6 (54)).

In reference to claim 11, Gardner teaches the semiconductor layer has a first and second surface (Fig.1 (40 has a top and bottom);

The trench is in the second surface(Fig.3 (46)); and

The semiconductor component further comprises a second region in the semiconductor region at the second surface of the layer having the first conductivity type and contiguous with the trench (Fig. 7 (60)- source region).

In reference to claim 12, Gardner teaches wherein:

the semiconductor layer has a first and second surface (Fig.1 (40 has a top and bottom);

The trench is in the second surface (Fig.3 (46)); and

The control electrode overlaps the second surface (Fig.6 (54)).

In reference to claim 13, Gardner teaches further comprising a second region in the semiconductor layer at the second surface having the first conductivity type, and adjacent to and non-contiguous with the trench (Fig.7 (56- source)).

In reference to claim 14, Gardner teaches wherein the trench extends into the semiconductor layer deeper than the channel (Fig.12 and Col.8, lines: 34-36).

In reference to claim 15, Gardner teaches wherein the channel region is absent underneath the trench (Col.8, lines: 34-36).

In reference to claim 16, Gardner teaches wherein the first region is absent underneath the trench (Fig.12 (60 and 66).

In reference to claim 17, Gardner teaches wherein the portion of the semiconductor layer is under the trench (Fig.12 (40).

In reference to claim 18, Gardner teaches wherein:

The semiconductor layer has a first surface and a second surface (Fig.2 (40)- has a top and bottom);

A first portion of the first region is at the first side of the trench and extends along a height of the semiconductor layer form the first surface toward the second (Fig.12 (60 and 66));

A second portion of the first region is at the second side of the trench and extends along the height of the layer form the first toward the second (Fig.12 (60 and 66)- each side of the trench);

The portion of the semiconductor layer is located between the first and second portions of the first region (Fig.12).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1500.

Carl Whitehead Jr.

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

LMS
December 1, 2002